

REMARKS/ARGUMENTS

The office action mailed on October 20, 2011, has been reviewed and carefully considered. Reconsideration is respectfully requested.

Claim Rejections - 35 U.S.C. §112

In the office action (page 2), claim 3 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The applicant has amended the recitation "the other flash chip" to read "said another one flash chip", and thus believes that the defects the examiner indicated have been removed.

Claim Rejections - 35 U.S.C. §103

In the office action (page 3), claims 1, 3, 6 and 7 are rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 6081878 (Estakhri) (herein after referred to as Estakhri) in view of U.S. Patent No. 5671439 (Klein) (herein after referred to as Klein).

In Claim 1 is a data write-in method for a flash memory, wherein the flash memory comprises at least two flash chips and a controller. The method of claim 1 comprises the following features:

A) partitioning physical blocks in the at least two flash chips such that the physical blocks in one of the at least two flash chips have odd logical block addresses and the physical blocks in another one of the at least two flash chips have even logical block addresses;

B) the controller receiving a data write-in instruction and analyzing a beginning logical address for writing from the received data write-in instruction;

C) the controller obtaining the logical block address needed to be written according to the analyzed beginning logical address;

D) the controller determining a parity of the obtained logical block address, and selecting one flash chip from the flash chips according to the determined parity of the logical block address;

E) the controller directing a first programming or erasing instruction to the physical blocks corresponding to the obtained logical block address in the selected flash chip;

F) the controller detecting whether said another one flash chip needs to be programmed or erased while the first programming or erasing instruction are being processed; if programming or erasing is needed in said another one flash chip, the method further comprises:

G) the controller directing a second programming or erasing instruction to said another one flash chip of at least two flash chips.

As mentioned in response to the previous office action, claim 1 refers to a chip interleaving method, i.e., the interleaving occurs between the chips and all of blocks in one chip shall have even logical addresses and the blocks in the other chip shall have odd addresses.

In the office action, the examiner alleges that Estakhri et al. discloses at least two flash chips and a controller. According to the examiner's comments, the applicant understands that the examiner believes Estakhri et al. fails to disclose the above features A)-G) . Nevertheless, the Office goes on to alleged that those skilled in the art would use the interleaving method described by Klein et al in the flash memory of Estakhri et al. so as to obtain the solution of claim 1 of the present application. The applicant respectfully disagrees.

1 The Examiner's Assertion is Hindsight

The applicant submits that, **without receiving the solution of the present application**, those skilled would not take the claimed features, i.e. the features A)-G), and apply them to the two flash chips and a controller of Estakhri et al to obtain claim 1 of the present application, especially considering that all Estakhri et al is alleged to disclose is two flash chips and a controller. Moreover, the Office action does not establish why one of ordinary skill in the art would apply the features A-G to Estakhri et al. The rationale submitted in the Office action on page 6 is a generic rationale that Estakhri et al at best discloses is an advantage exclusive to its own method. The Office action does not even attempt to apply its rationale to the actual asserted combination. In this sense, the applicant humbly submits the Examiner's assertion is hindsight.

2. Klein's Solution is not Applicable to the Flash

Claim 1 of the present application refers to a chip interleaving method, i.e., the interleaving occurs between the chips and all of blocks in one chip shall have even logical addresses and the blocks in the other chip shall have odd addresses. In particular, the controller directs a first programming or erasing instruction to the physical blocks corresponding to the obtained logical block address in the selected flash chip, and detects whether said another one flash chip needs to be programmed or erased while the first programming or erasing instruction are being processed. If programming or erasing is needed in said another one flash chip, he controller directs a second programming or erasing instruction to said another one flash chip of at least two flash chips. It should be understood for those skilled in the art that, each of the flash chips has the lines for transferring the data and the address, and the lines of each chip may be coupled to the controller. During the operation, the lines for the both chips may have the signal. Accordingly, the two chips can be **simultaneously** written or read.

In the contrast, according to Klein, the data and the address are transferred trough different courses or procedures, i.e. a phase of access and a phase of xfer. In particular, the drives A and B load the data therein onto the on-board memory (the phase of access), and then transfers the data from the on-board memory to the host (the phase of xfer). That is, during the phase of xfer, drive B must have to wait until the operation on drive A is finished, vice versa. Please refer to Lines 5-10 of Colum 7 and Line 60 of Colum 7 to Line 10 of Colum 8.

Moreover, from Fig. 7 of Klein, it can be seen that the data and the address are transferred trough different channels. In particular, although Klein discloses "*driver 60 includes a pair of first-in/first out (FIFO) registers 72 and 74, which enables data transfer to be performed with multiple physical devices at the same time*", please refer to Lines 45-49 in Colum 16 of the description, it does not mean that Klein could simultaneously write or read drive A and drive B. Specifically, as shown in Fig. 7 and disclosed in Lines 65-67 in Colum 16 of the Description, a bus master 65 drives the FIFO register 72 through Lines 91 and 92, while drives the FIFO register 74 through Lines 93 and 94. The bus master 65 then determines which drive to be written, drive A or drive B? However, all the data are transferred through "Data Path" 70, which means it is impossible to simultaneously write drive A and drive B.

In addition, it is true that Klein mentions the contents in regard to the flash, but fails to give any specific data write-in method in flash. Due to the inherent characteristics of the flash as mentioned in the Background of the subject application, the solution of Klein is not applicable to the flash.

3. The Advantages of Claim 1 of the Present Application

Klein refers to a writing method between the host and the peripheral devices, and the controlling thereof incurs between the host and the peripheral devices as well. Accordingly, Klein needs to revise or improve the hardware of the host. However, the solution of claim 1 of the present application refers to a data write-in method within a flash memory, and does not need to revise or improve the hardware of the host. Accordingly, there is no reason for one to apply the teachings of Klein to the claimed data write-in method for a flash memory comprising at least two flash chips and a controller.

4. Conclusion

In view of the above, **the method as disclosed by Klein et al is different from the chip interleaving method as claimed in claim 1 of the present application.** Accordingly, it is impossible for those skilled in the art to use the method of Klein et al in the two flash chips and a controller of Estakhri et al to obtain the solution of claim 1 of the present application. **And there is no motivation for the skilled to modify the method of Klein et al and then apply the modified method to the chips and a controller of Estakhri et al.** Accordingly, claim 1 is not obvious over Estakhr et al in view of Klein et al.

In addition, claims 3, 6 and 7 are not obvious over Estakhr et al in view of Klein et al, too, at least because they depend on claim 1 and recite all the limitations of claim 1. Withdrawal of the rejection of claims 1, 3, 6 and 7 under 35 U.S.C. § 103 is respectfully requested.

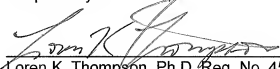
For the reasons set forth above, the applicant respectfully submits that claims 1, 3, 6 and 7 pending in this application are in condition for allowance over the cited

references. Accordingly, the applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an indication of allowable subject matter.

This amendment is considered to be responsive to all points raised in the office action. Should the examiner have any remaining questions or concerns, the examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve those concerns.

Respectfully submitted,

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